R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a method of conditional branching in a pipelined processor. The method generally comprises the steps of (A) fetching a first instruction stored at a branch target address in response to encountering a branch instruction at a program counter address, (B) decoding a second instruction stored at a next address adjacent the program counter address substantially simultaneously with the fetching and (C) evaluating between (i) taking a branch defined by the branch instruction and (ii) not taking the branch substantially simultaneously with the fetching.

SUPPORT FOR THE DRAWING AMENDMENTS

Support for the drawing amendments can be found in the specification, for example, on page 6 lines 4-13 and page 7 lines 7-19, as originally filed. Thus, no new matter has been added.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments and the new claims may be found in the specification, for example, on page 4 lines 10-17, page 5 lines 3-6, page 5 lines 17-21, page 7 lines 12-17, page 8

lines 4-16, page 9 lines 5-18, page 10 lines 7-9 and FIGS. 2 and 3, as originally filed. Thus, no new matter has been added.

DRAWING OBJECTION

The objection to the drawings has been obviated by appropriate amendment and should be withdrawn. A box has been added to each of the FIGS. 1 and 2 to identify the portion of system referenced by arrow 100 as suggested by the Examiner.

SPECIFICATION OBJECTIONS

The objection to the headings is respectfully traversed. 37 C.F.R. 1.77(c) uses the open language "should", not closed language like "must". Therefore, the rejection should be withdrawn.

The objection to the title is respectfully traversed and should be withdrawn. The present title is descriptive. Furthermore, the proposed title suggests using "algorithm" to describe the invention. Since algorithms are not normally considered statutory subject matter, the proposed title appears less descriptive of the present invention.

CLAIM OBJECTION

The objection to the claims has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claim 9 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-2, 7-8 and 14 under 35 U.S.C. §102 as being anticipated by Moyer '678 has been obviated by appropriate amendment and should be withdrawn.

Moyer concerns a method and apparatus for controlling conditional branch execution in a data processor (Title). Moyer does not appear to disclose or suggest every element as arranged in the claims. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 1 provides (A) fetching a first instruction stored at a branch target address, (B) decoding a second instruction and (C) evaluating between (i) taking a branch defined by a branch instruction and (ii) not taking the branch substantially simultaneously. In contrast, Moyer appears to be silent regarding decoding a second instruction while simultaneously fetching an instruction at a branch address and evaluating a branch condition of a branch instruction. Therefore, Moyer does not appear to disclose or suggest (A) fetching a first instruction stored at a branch target address, (B) decoding a second instruction and (C)

evaluating between (i) taking a branch defined by a branch instruction and (ii) not taking the branch substantially simultaneously as presently claimed. Claim 14 contains language similar to claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 7 provides a circuit presenting (i) a branch target address based on a branch instruction stored at a program counter address, (ii) a sequential instruction address having a value adjacent the program counter address and (iii) a mispredict recovery address to a multiplexer substantially simultaneously. In contrast, Moyer appears to be silent regarding three addresses presented to a multiplexer 24 (FIG. 1) substantially simultaneously. Therefore, Moyer does not appear to disclose or suggest presenting (i) a branch target address based on a branch instruction stored at a program counter address, (ii) a sequential instruction address having a value adjacent the program counter address and (iii) a mispredict recovery address to a multiplexer substantially simultaneously as presently claimed. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 3-6, 9-10 and 12-13 under 35 U.S.C. §103(a) as being unpatentable over Moyer in view of Hennessy's book has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 11 under 35 U.S.C. §103(a) as being unpatentable over Moyer in view of Hennessy and Eckner '460 has been obviated by appropriate amendment and should be withdrawn

Claims 3-6 and 9-13 depend, either directly or indirectly, from the independent claims which are now believed to be allowable. As such, claims 3-6 and 9-13 are fully patentable over the cited references and the rejections should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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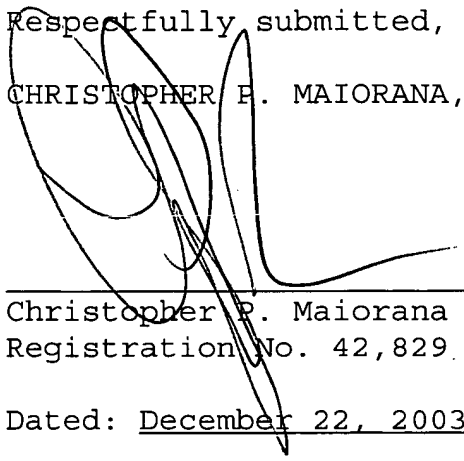

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Dated: December 22, 2003

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Docket No.: 00-419 / 1496.00055